

Model Name: GA-P55M-UD2 1.0

SHEET TITLE

01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU LGA1156-A
05	CPU LGA1156-B
06	CPU LGA1156-C
07	DDR III CHANNEL A
08	DDR III CHANNEL B
09	DDR III POWER CAP
10	PCI EXPRESS*16 SLOT
11	PCH FDI,DMI,USB,PCIE,NVRAM
12	PCH DP,CLK BUFFER
13	PCH HOST,SATA,PCI
14	PCH GPIO,CTRL,AUDIO
15	PCH PWR,GND
16	PCI EXPRESS*4 SLOT
17	PCI EXPRESS*1 SLOTS X3
18	PCI SLOT X2
19	ITE 8720 LPC IO
20	COM, -PROHOT , DYNAMIC OC , LPT
21	Dual BIOS
22	ALC888/889A
23	REAR AUDIO JACK
24	CLOCK GEN ICS9LPRS914
25	VCORE PWM ISL6334CR-1
26	VCORE PWM ISL6334CR-2
27	DISCRETE POWER I

SHEET TITLE

28	DDR 15V & VCC1 05 PCH PWM ISL6545CBZ
29	CPU VAXG PWM ISL6314CRZ
30	CPU VTT PWM ISL6322G
31	F PANEL , F USB , FDD
32	ATX POWER
33	Marvell 88SE9123
34	REALTEK RTL8111DL
35	REALTEK RTL8111DL 1
36	TI TSB43AB23 1394
37	HWM,KB/MS , FAN CTRL
38	TPM SLB9635TT
39	ESATA JMB362
40	TABLE LIST
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GA-P55M-UD2 Version: 1.0

Component value change history

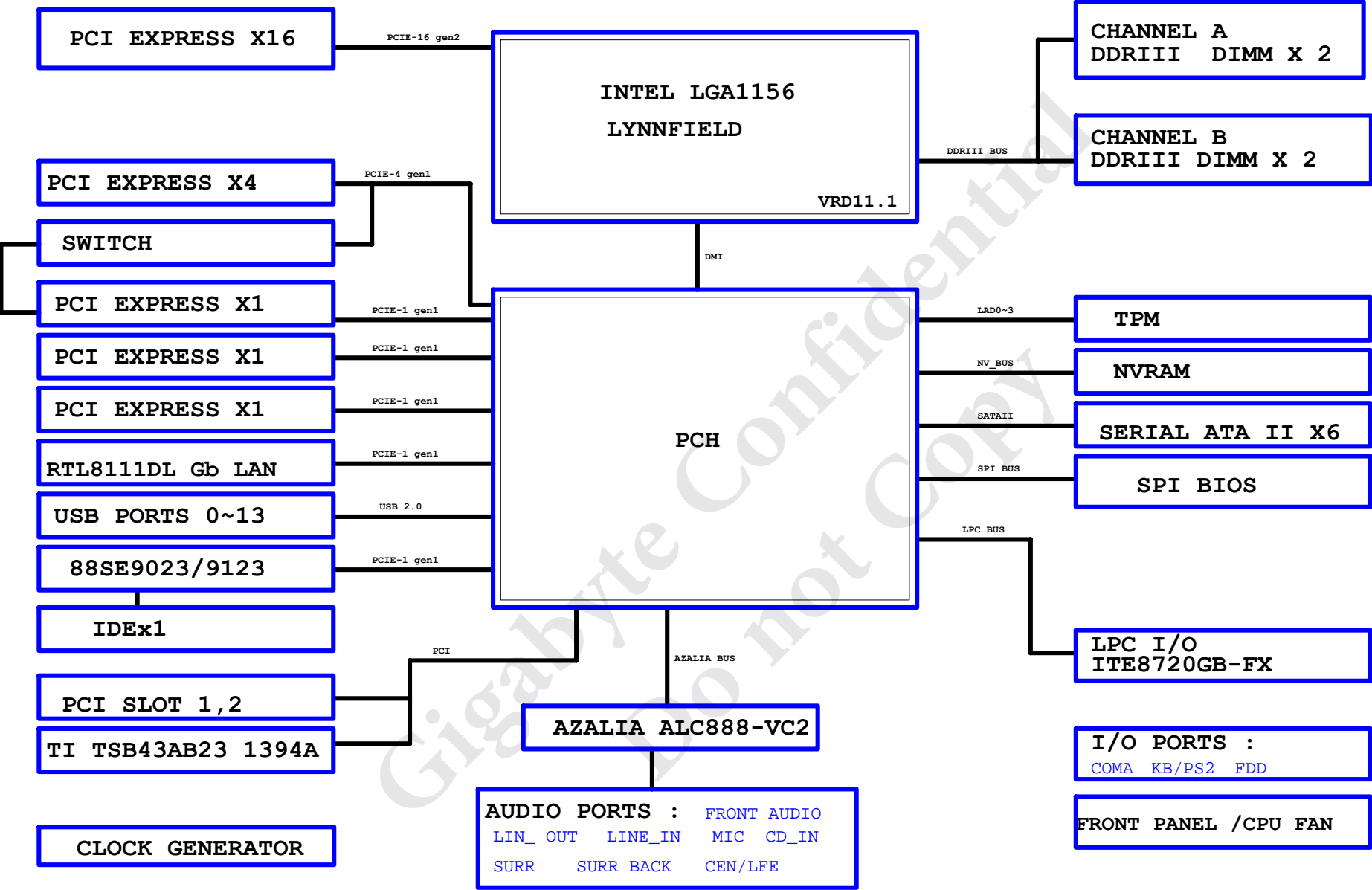
Data	Change Item	Reason
0.1	1. 9ME55QD3R-00-01	
EP55A-UD3P 0.1	1. Add R687,BC241 For ISL8014 VDD PIN	
	2. IDE Conn. change 直立式	
	3. ADD CPU RM	
	4. CPU_VAXG R153 --> R151 68K/4/1 , R127 20K/4/1 --> 42K/4/1 , BC60 0.1u --> 1n/4	
	5. DIMM & LPT COLOR --> BLUE	
	6. REMOVE 7474 , CHANGE TO ITE8720/JX	
	7. CLK阻值調整	
	8. PCIEX16 CHANGE TO RIGHT EJECTOR	
	9. 0.5uH --> 1.0uH 含阻值修改	
EP55A-UD3P 0.2	1. CHECK +12V SHORT PAD FOR 10mil	
	2. F1_1394加蓋(包材階)	
	3. ADD DR86=124K/4/1 , DR88=249K/4/1	
	4. U12~U15 upi6262M --> upi6267M	
	5. DRAM_PWROK R490=1K/4/1 , R491=3K/4/1	
	6. REMOVE DR138=0/4 , ADD DR139,DR141=0/4	
	7. RU2指定料號:10HP4-112540-11R	
	8. 排阻指定廠牌用WALSIN	
	9. LU1,LU4 RTL8111D --> RTL8111C	
	10. PCB "育富"移除	
	11. ONFI指定用11SML-600078-02R	
	12. R376 2.26K/4/1 --> 2.55K/4/1	
	13. 確認上哪種upi6262 10%/upi6267?	
	14. FB7~FB10 REMOVE	
	15. PCH BUFFER 25MHz REMOVE "X2,C93,C94,R420"	
	16. BIOS 16M --> 32M (FOR ONFI ONBOARD)	
		10B 1. ADD R190 1K/4/1 FOR PCI-E OVER-CLOCK
P55M-UD4	1. RTL8111C --> RTC8111D (是否上新板VB?)	
P55M-UD2 0.2	1. ADD PACKAGE F1 1394 2. P55 REV.B1 --> REV.B2 3. VCC1_05_PCH --> OP+MOS	
P55M-UD2 1.0	1. CHECK POWER SEQUENCY FOR VCC1_05_PCH 2. PROCHOT阻值修改 3. REMOVE PLL 22U 4. Q73,Q74 UPA2724 --> UPA2726	

Circuit or PCB layout change
for next version

DATE	Change Item	Reason
EP55-UD3R 0.1	1. 9ME55QD3R-00-01	
EP55A-UD3P 0.1	1. FWR_LED GPIO46 --> GPIO20	
	2. CHECK DDR3 LAYER RULE UPDATE (DDR3 LIBRARY UPDATE)	
	3. ADD F_PANEL RESET & BOTTOM ESD PROTECT	
	4. CPU ISENSE & IOUT ADD CONTROL CIRCUIT	
	5. RESET 7474 COST DOWN CHECK	
	6. SRCCLK_CKG TRACE CHANGE TO TOP	
	7. USBP12 , USBP13 +- SWAP NET	
	8. +12V PROTECT Q91 ADD Damping Resistor "R748"	
	9. 零件位置BAT移出至BAT外框	
	10. X3與CLR_CMOS距離不足5mm	
	11. Remove 0 ohm	
	12. CPU_VTT ADD背面電容SBC9,SBC10	
	13. CPU_VTT ADD VTT_SENSE , VTT_VSS	
	14. MODIFY PCIEX4 & PCIEX1 SELECT "-4X_EN"	
	15. ADD ESATA JMB362	
	16. ITE8275 PATCH -SYS_RST 漏電	
	17. DRAM_PWROK 留Damping 電阻	
	18. DRIVER的PIN5 GND走線與GATE同粗	
	19. LAN CTRL18為PHASE須在第二層做隔離	
EP55A-UD3P 0.2	1. REMOVE AUDIO ESD	
	2. REMOVE CPU_VAXG	
	3. PCH_CLK 改 SHORT PAD (0 ohm維持10pcs以下)	
	4. ITE8275 GPIO11,GPIO13 TO TURBO0/TURBO1	
	5. F_PANEL UPDATE H2X10PANEL-1	
	6. ONFI 改 ON BOARD	
	7. 1394 "IEC1" NET SWAP & SHORT PROTECT	
	8. PIN HEATER CHECK	
	9. ITE8275 SYS_RST PATCH	
	10. BC118,BC119 --> TBC29,TBC30	
	11. BC5靠近M_BIOS PIN8 , BC6靠近M_BIOS PIN8	
	12. U2 7474 REMOVE	

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BLOCK DIAGRAM

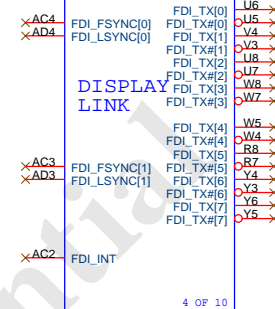


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FDI : 16/5/5/16(breakout min 8/4/5/4/8)

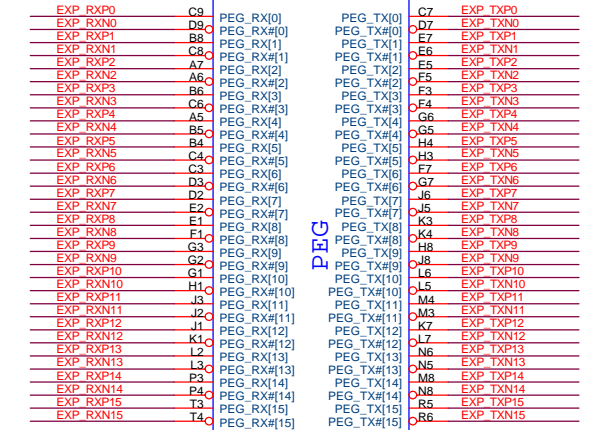
LGA1156D

Impedance=80 +- 17.5%



LGA1156[10SC1-F01156-01R]

EXP_TXP0.15I >> EXP_TXP0.15] (15)
EXP_TXN0.15I >> EXP_TXN0.15] (15)
EXP_RXP0.15I >> EXP_RXP0.15] (15)
EXP_RXN0.15I >> EXP_RXN0.15] (15)

PCIEX16:16/5/5/16(breakout min 8/4/5/4/8)
Impedance=80 +- 17.5%

LGA1156C

PEG

DMI

DMI:12/5/5/12
Impedance=80 +- 17.5%

(10) DMI_0RX0 >> DMI_0RXN (10)
(10) DMI_0RXN >> DMI_0RXN (10)
(10) DMI_1RX0 >> DMI_1RXN (10)
(10) DMI_1RXN >> DMI_1RXN (10)
(10) DMI_2RX0 >> DMI_2RXN (10)
(10) DMI_2RXN >> DMI_2RXN (10)
(10) DMI_3RX0 >> DMI_3RXN (10)
(10) DMI_3RXN >> DMI_3RXN (10)

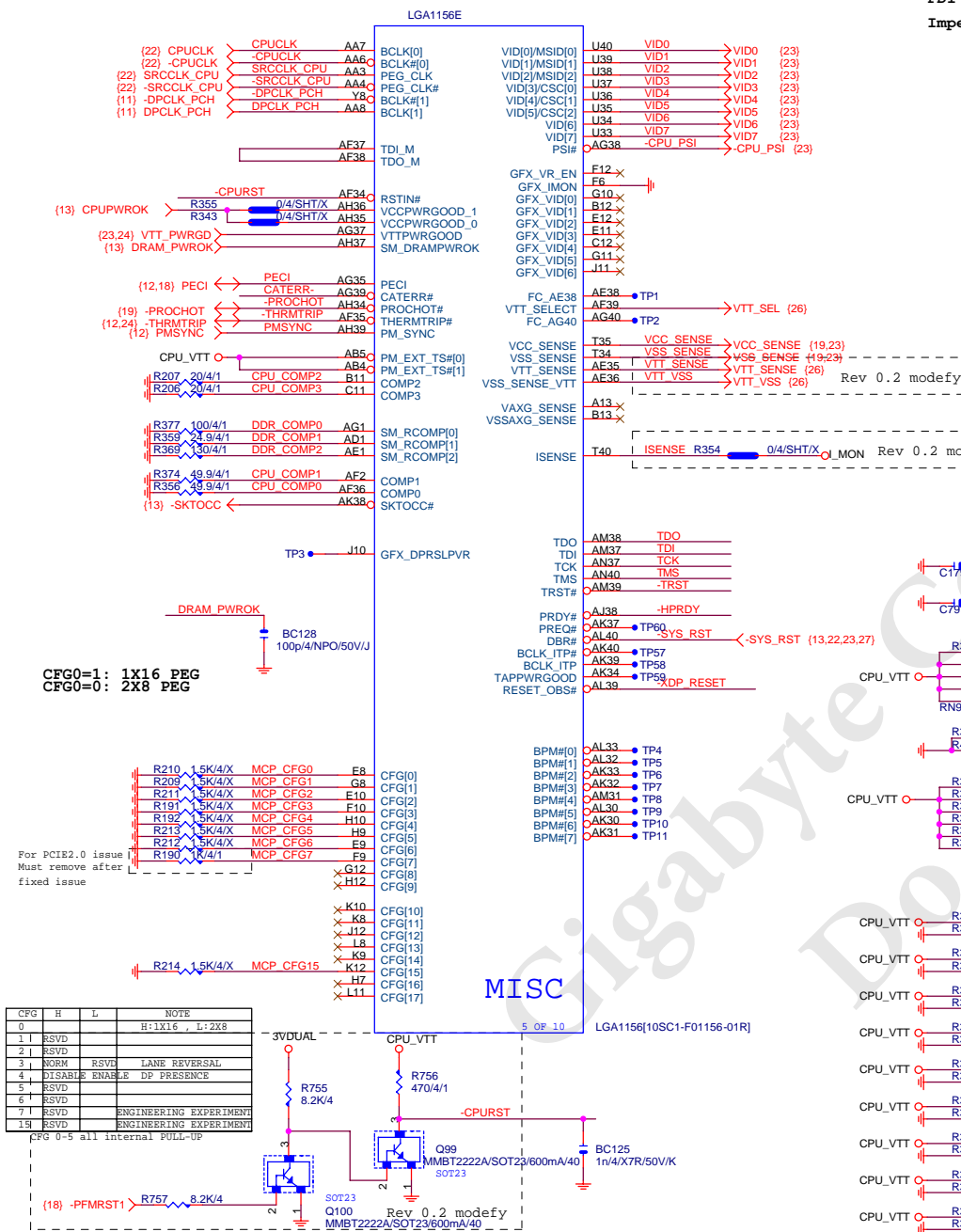
POWER ON CONFIG TABLE (Default=1.2250V)

	FUNCTION	DEFAULT
VID0	MSI0	0
VID1	MSI1	1
VID2	MSI2	1
VID3	IMON CFG0	1
VID4	IMON CFG1	1
VID5	IMON CFG2	1
VID6	RSVD	
VID7	VRD SEL	LOW
PSI#	RSVD	LOW

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MAAA0	AW18	SA_MA[0]	SA_DQS[0]	AK3	DQSA0
MAAA1	AY15	SA_MA[1]	SA_DQS[1]	CA13	-DQSA0
MAAA2	AV15	SA_MA[2]	SA_DM[0]	CA12	DMA0
MAAA3	AU15	SA_MA[3]		AH1	MDA0
MAAA4	AW14	SA_MA[4]	SA_DQ[0]	AJ4	MDA1
MAAA5	AY13	SA_MA[5]	SA_DQ[1]	AL2	MDA2
MAAA6	AV14	SA_MA[6]	SA_DQ[2]	AL1	MDA3
MAAA7	AW13	SA_MA[7]	SA_DQ[3]	AG2	MDA4
MAAA8	AU14	SA_MA[8]	SA_DQ[4]	AH2	MDA5
MAAA9	AW12	SA_MA[9]	SA_DQ[5]	AK1	MDA6
MAAA10	AT19	SA_MA[10]	SA_DQ[6]	AK2	MDA7
MAAA11	AU13	SA_MA[11]	SA_DQ[7]		
MAAA12	AW11	SA_MA[12]		AP2	DQSA1
MAAA13	AU24	SA_MA[13]	SA_DQS[11]	AP3	-DQSA1
MAAA14	AT11	SA_MA[14]	SA_DQS[11]	AN1	DMA1
MAAA15	AR10	SA_MA[15]	SA_DM[1]		
(7) -SWEA	-SWEA	AT22	SA_WE#	AN3	MDA8
(7) -SCASA	-SCASA	AU22	SA_CAS#	AN2	MDA9
(7) -SRASA	-SRASA	AT20	SA_RAS#	AR3	MDA10
(7) SBAA0	SBAA0	AV20	SA_BS[0]	AR2	MDA12
(7) SBAA1	SBAA1	AU19	SA_BS[1]	AM3	MDA11
(7) SBAA2	SBAA2	AU12	SA_BS[2]	AM2	MDA13
(7) -CSA0	-CSA0	AV21	SA_CS[0]	AP1	MDA14
(7) -CSA1	-CSA1	AW24	SA_CS[1]	AR4	MDA15
(7) -CSA2	-CSA2	AU21	SA_CS[2]		
(7) -CSA3	-CSA3	AU23	SA_CS[3]	AL4	DQSA2
(7) CKEA0	CKEA0	AU10	SA_CKE[0]	SA_DQS[2]	SA_DM[2]
(7) CKEA1	CKEA1	AW10	SA_CKE[1]	AT4	MDA16
(7) CKEA2	CKEA2	AV10	SA_CKE[2]	AJ2	MDA17
(7) CKEA3	CKEA3	AY10	SA_CKE[3]	AW3	MDA18
MODT_A0	AV23	SA_ODT[0]	SA_DQ[19]	AW4	MDA19
MODT_A1	AV24	SA_ODT[1]	SA_DQ[20]	AT3	MDA20
MODT_A2	AW23	SA_ODT[2]	SA_DQ[21]	AT1	MDA21
MODT_A3	AY24	SA_ODT[3]	SA_DQ[22]	AV2	MDA22
			SA_DQ[23]	AV4	MDA23
(7) DCLKA0	DCLKA0	AR22	SA_CK[0]	AY6	DQSA3
(7) -DCLKA0	-DCLKA0	AR21	SA_CK[0]	SA_DQS[3]	SA_DM[3]
(7) DCLKA1	DCLKA1	AP18	SA_CK[1]	AY5	MDA24
(7) -DCLKA1	-DCLKA1	AN18	SA_CK[1]	AY5	MDA25
(7) DCLKA2	DCLKA2	AN21	SA_CK[2]	AJ8	MDA26
(7) -DCLKA2	-DCLKA2	AP21	SA_CK[2]	AY8	MDA27
(7) DCLKA3	DCLKA3	AP19	SA_CK[3]	AY5	MDA28
(7) -DCLKA3	-DCLKA3	AN19	SA_CK[3]	AY6	MDA29
(7,8) -DDR3_RST	-DDR3_RST	AV8	SM_DRAMRST#	SA_DQ[30]	AW7
TP1	AK22	SA_CS#4	SA_DQS[4]	AR28	DQSA4
TP1	AL23	SA_CS#5	SA_DQS[5]	CA129	-DQSA4
TP1	AK23	SA_CS#6	SA_DM[4]	AN29	DMA4
				AN27	MDA32
				AT28	MDA33
				SA_DQ[32]	SA_DQ[33]
				SA_DQ[34]	AP28
				SA_DQ[35]	AP30
				SA_DQ[36]	AN26
				SA_DQ[37]	AR27
				SA_DQ[38]	AN30
				SA_DQ[39]	MDA39
				AV32	DQSA5
				CAW32	-DQSA5
				AW31	DMA5
				AL30	MDA40
				AL31	MDA41
				SA_DQ[40]	SA_DQ[41]
				SA_DQ[42]	SA_DQ[43]
				SA_DQ[44]	SA_DQ[45]
				SA_DQ[46]	SA_DQ[47]
				AW33	MDA46
				AW33	MDA47
				AW36	DQSA6
				CAU35	-DQSA6
				SA_DM[6]	SA_DM[6]
				AW35	MDA48
				AY35	MDA49
				SA_DQ[48]	SA_DQ[49]
				SA_DQ[50]	SA_DQ[51]
				SA_DQ[52]	SA_DQ[53]
				SA_DQ[54]	SA_DQ[55]
				AW37	MDA55
				AP38	DQSA7
				CA138	-DQSA7
				AT38	DMA7
				SA_DM[7]	
				AT39	MDA56
				AT40	MDA57
				AN38	MDA58
				AN39	MDA59
				SA_DQ[56]	SA_DQ[57]
				SA_DQ[58]	SA_DQ[59]
				SA_DQ[60]	SA_DQ[61]
				SA_DQ[62]	SA_DQ[63]
				AP39	MDA62
				AP40	MDA63

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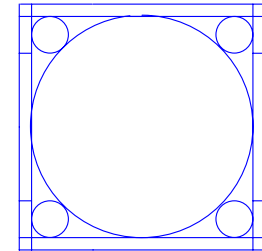
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MAAB0	AU20	SB_MA[0]	SB_DQS[0]	AF4	DQSB0
MAAB1	AU18	SB_MA[1]	SB_DQS[1]	AE5	-DQSB0
MAAB2	AV18	SB_MA[2]	SB_DM[0]	AE4	DMB0
MAAB3	AU17	SB_MA[3]		AD7	MDB0
MAAB4	AY18	SB_MA[4]	SB_DQ[0]	AD6	MDB1
MAAB5	AV17	SB_MA[5]	SB_DQ[1]	AH8	MDB2
MAAB6	AW17	SB_MA[6]	SB_DQ[2]	AJ8	MDB3
MAAB7	AU16	SB_MA[7]	SB_DQ[3]	AC7	MDB4
MAAB8	AT17	SB_MA[8]	SB_DQ[4]	AC6	MDB5
MAAB9	AY25	SB_MA[9]	SB_DQ[5]	AE5	MDB6
MAAB10	AW16	SB_MA[10]	SB_DQ[6]	AE6	MDB7
MAAB11	AW15	SB_MA[11]		AH6	DQSB1
MAAB12	AW18	SB_MA[12]	SB_DQS[11]	AE5	-DQSB1
MAAB13	AY12	SB_MA[13]	SB_DQS[11]	AH4	DMB1
MAAB14	AV11	SB_MA[14]	SB_DM[1]	AG5	MDB8
MAAB15	AV11	SB_MA[15]	SB_DM[1]	AH7	MDB9
(8) -SWEB	-SWEB	AU26	SB_WE#	AK6	MDB10
(8) -SCASB	-SCASB	AW26	SB_CAS#	AL4	MDB11
(8) -SRASB	-SRASB	AW26	SB_RAS#	AL4	MDB12
(8) SBAB0	SBAB0	AU25	SB_BS[0]	AL6	MDB13
(8) SBAB1	SBAB1	AW25	SB_BS[1]	AL7	MDB14
(8) SBAB2	SBAB2	AV12	SB_BS[2]	AK7	MDB15
(8) -CSB0	-CSB0	AY27	SB_CS[0]	AN6	DQSB2
(8) -CSB1	-CSB1	AW26	SB_CS[1]	AM6	-DQSB2
(8) -CSB2	-CSB2	AV26	SB_CS[2]	AM7	DMB2
(8) -CSB3	-CSB3	AV26	SB_CS[3]	AL6	MDB16
(8) CKEB0	CKEB0	AW8	SB_CKE[0]	AN5	MDB17
(8) CKEB1	CKEB1	AV9	SB_CKE[1]	AP6	MDB18
(8) CKEB2	CKEB2	AU9	SB_CKE[2]	AR5	MDB19
(8) CKEB3	CKEB3	AV9	SB_CKE[3]	AL5	MDB20
MODT_B0	AU27	SB_ODT[0]	SB_DQ[20]	AN4	MDB21
MODT_B1	AU29	SB_ODT[1]	SB_DQ[21]	AN7	MDB22
MODT_B2	AV27	SB_ODT[2]	SB_DQ[22]	AP5	MDB23
MODT_B3	AU28	SB_ODT[3]	SB_DQ[23]	AR8	DQSB3
			SB_DQS[3]	AP8	-DQSB3
			SB_DM[3]	AT7	DMB3
(8) DCLKB0	DCLKB0	AR17	SB_CK[0]	AT6	MDB24
(8) -DCLKB0	-DCLKB0	AR16	SB_CK[0]	AR7	MDB25
(8) DCLKB1	DCLKB1	AT15	SB_CK[1]	AR9	MDB26
(8) -DCLKB1	-DCLKB1	AR15	SB_CK[1]	AM8	MDB27
(8) DCLKB2	DCLKB2	AN17	SB_CK[2]	AN8	MDB28
(8) -DCLKB2	-DCLKB2	AN16	SB_CK[2]	AR6	MDB29
(8) DCLKB3	DCLKB3	AR19	SB_CK[3]	AL8	MDB30
(8) -DCLKB3	-DCLKB3	AR18	SB_CK[3]	AT9	MDB31
TP12	AM23	SB_CS#4	SB_CS[4]	AT25	DQSB4
TP13	AM24	SB_CS#5	SB_CS[5]	AR24	-DQSB4
TP15	AL24	SB_CS#6	SB_CS[6]	AN24	DMB4
TP17	AK24	SB_CS#7	SB_CS[7]	AN23	MDB32
				AP23	MDB33
				SB_DQ[32]	SB_DQ[33]
				SB_DQ[34]	SB_DQ[35]
				SB_DQ[36]	SB_DQ[37]
				SB_DQ[38]	SB_DQ[39]
				AP22	MDB36
				AP25	MDB37
				AT26	MDB38
				AT26	MDB39
				AP32	DQSB5
				AR32	-DQSB5
				AN32	DMB5
				AT32	MDB40
				AP31	MDB41
				AR33	MDB42
				AM32	MDB43
				AT31	MDB44
				AR31	MDB45
				AT34	MDB46
				AT33	MDB47
				AR36	DQSB6
				AR37	-DQSB6
				AM33	DMB6
				AR35	MDB48
				AT36	MDB49
				AN33	MDB50
				AP36	MDB51
				AP34	MDB52
				AT35	MDB53
				AN34	MDB54
				AP37	MDB55
				AL37	DQSB7
				AM36	-DQSB7
				AK35	DMB7
				AL35	MDB56
				AM35	MDB57
				AJ36	MDB58
				AJ37	MDB59
				AN35	MDB60
				AM34	MDB61
				AJ35	MDB62
				AL36	MDB63

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CR
CPU RETAIN/WX

Need check the new CPU ME

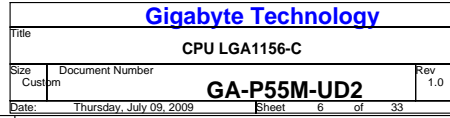
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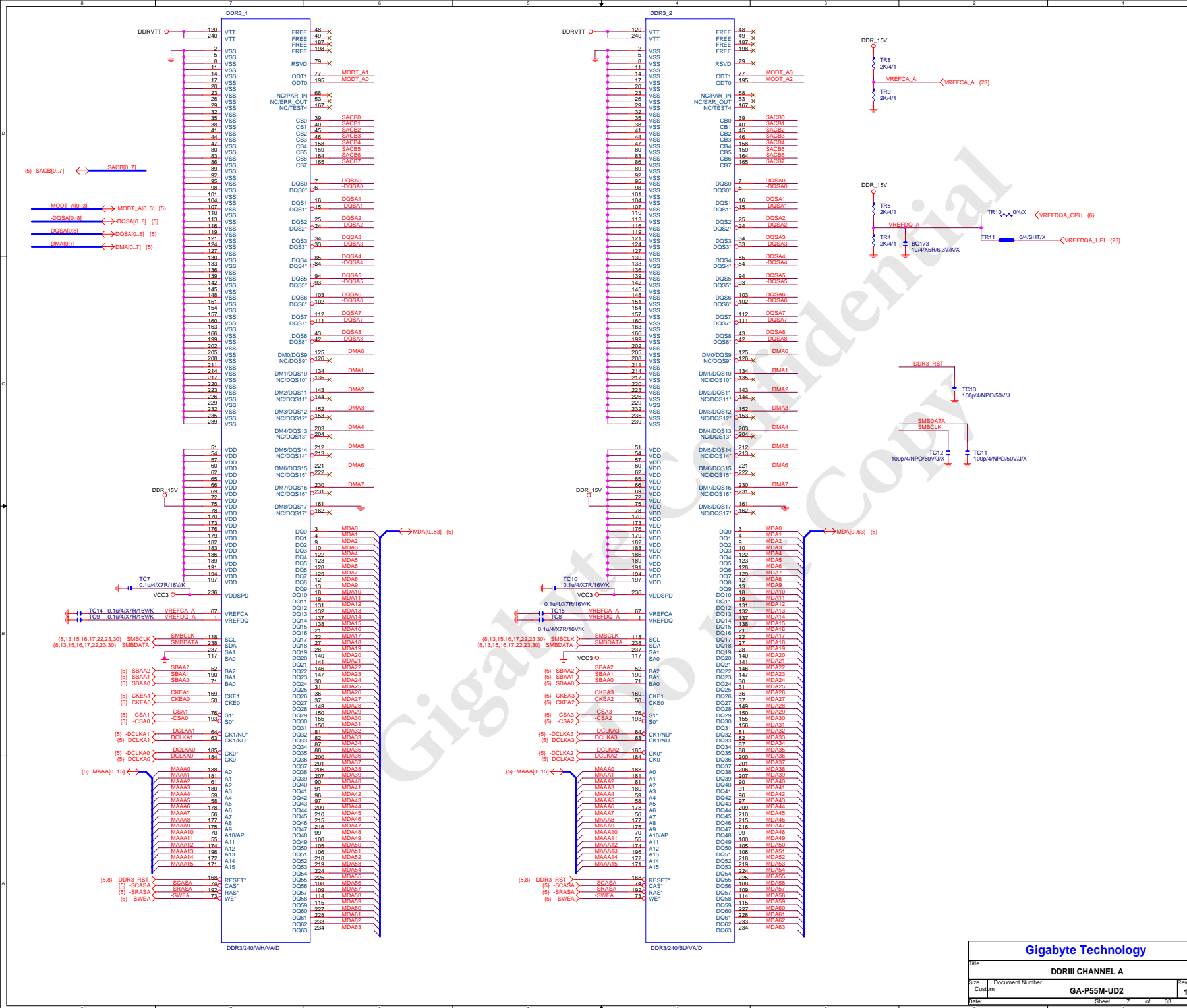


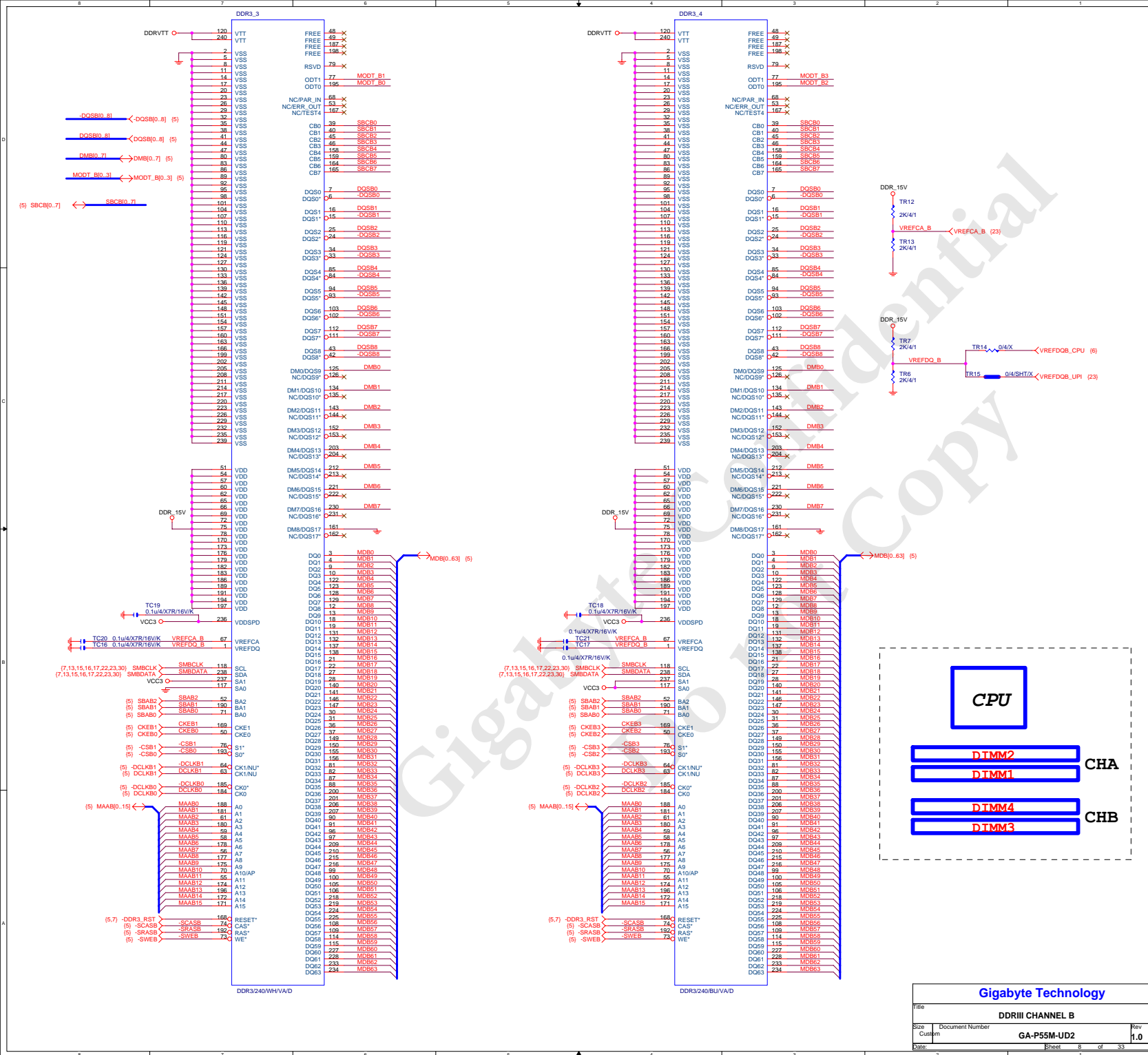
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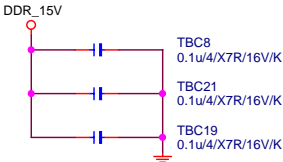




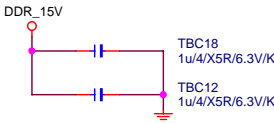
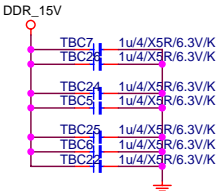
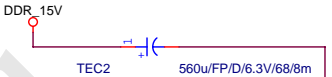
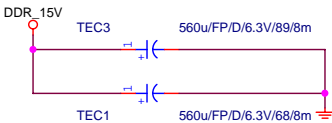
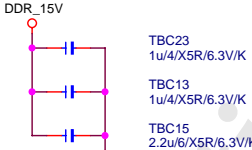
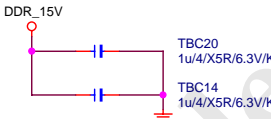
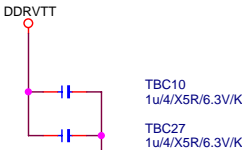
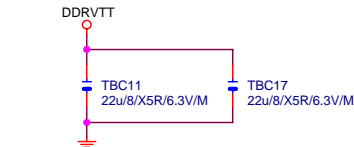
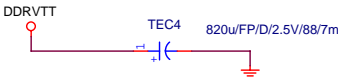
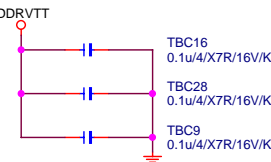


DDR TERMINATION
CHANNEL A/B

DDR15V Decouple

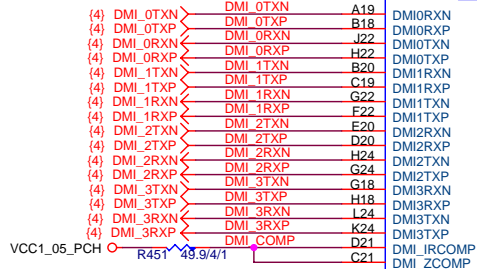


DDRVTT Decouple

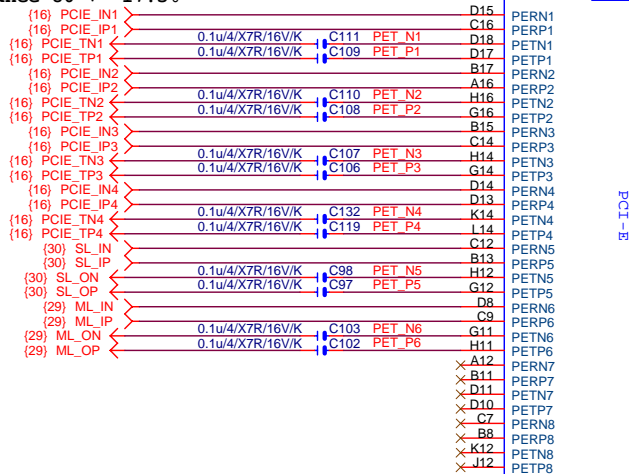


Gigabyte Technology			
Title			
DDRIII POWER CAP			
Size	Document Number	GA-P55M-UD2	Rev
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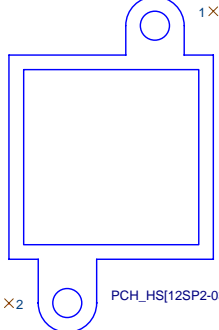
DMI:12/5/5/5/12
Impedance=80 +- 17.5%



PCIE X1 :15/5/5/5/15
Impedance=80 +- 17.5%



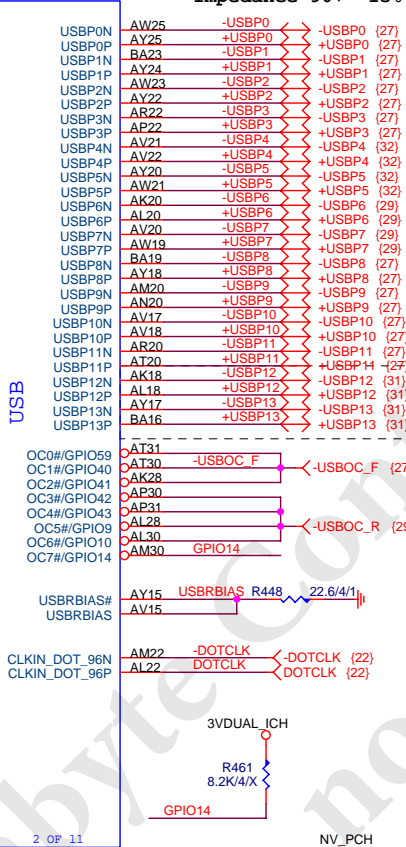
PCH_HS



USB OC#	Configure
OC0#	USB0,1
OC1#	USB2,3
OC2#	USB4,5
OC3#	USB6,7
OC4#	USB8,9
OC5_6#	USB10~13
OC7#	

PCHB

USB:15/4.5/7.5/4.5/15
Impedance=90+- 15%

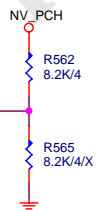


USB

PCI-E

2 OF 11

BD82P55-B2/S



NV_ALE
ble Danbury
able Danbury

Intel anti theft techonlogy

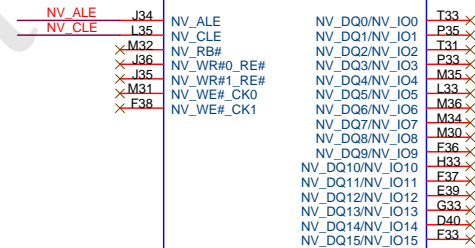
DMI Terminator voltage
HI : AC COUP : TX/RX TO VCC
LO : DC COUP : HALF SWING

Impedance=50+- 15%
ONFI: NV_DQ 4/5

NV_DQS 4/10

NV_CTRL 4/10

NV_CK 4/15

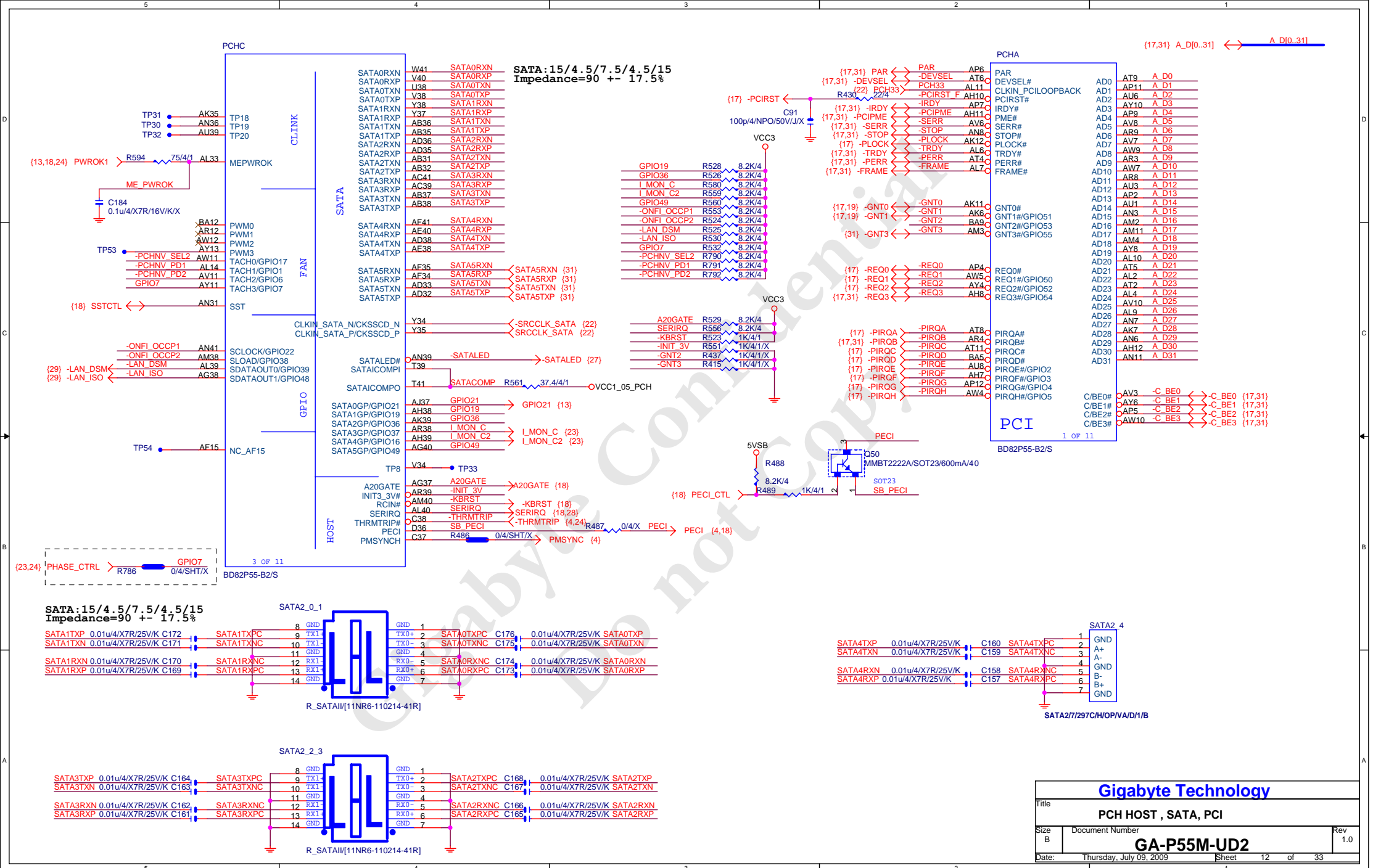


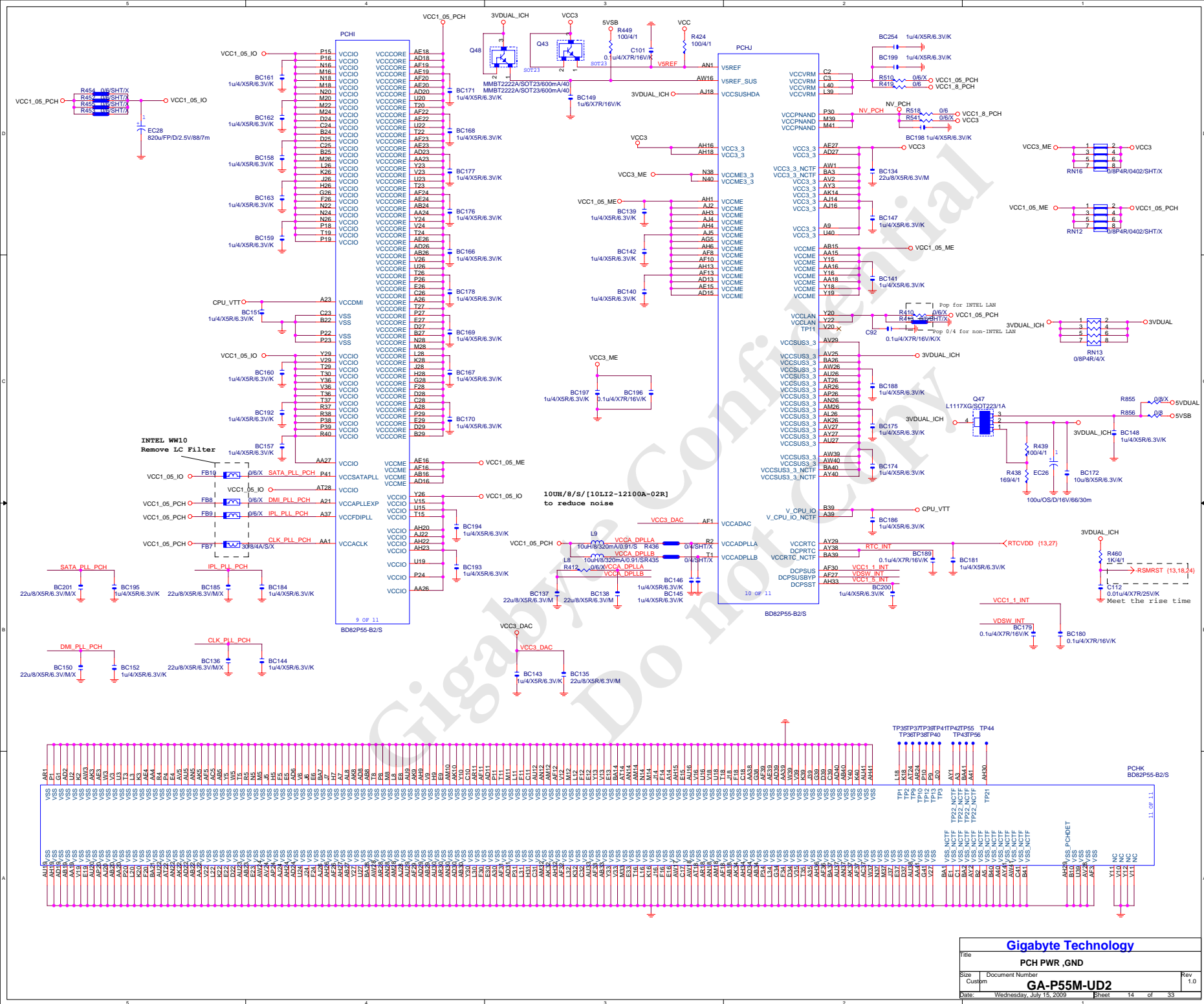
NVRAM

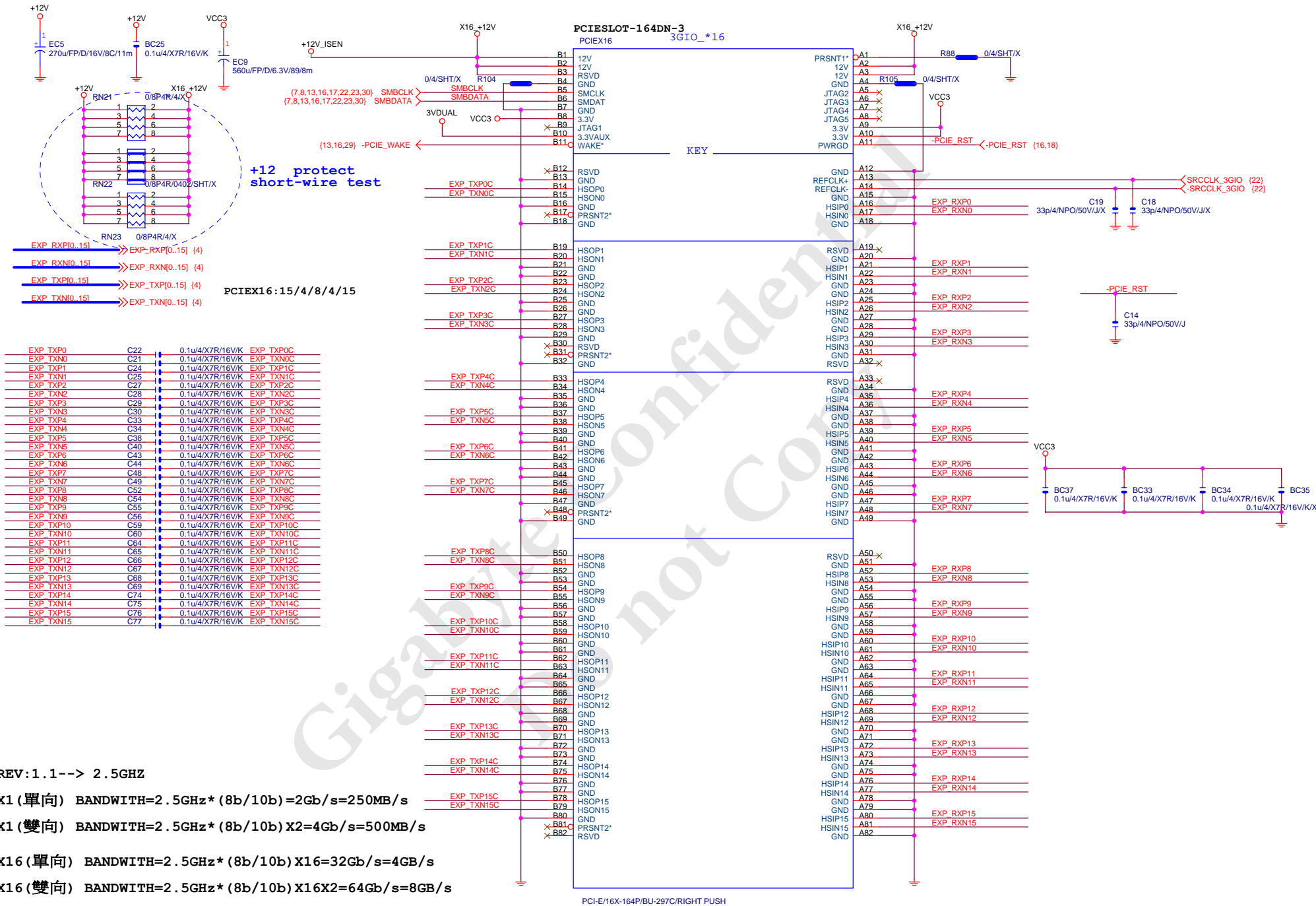
5 OF 11
BD82P55-B2/S

Gigabyte Technology

Title	PCH FDI,DMI,USB ,PCIE,NVRAM	Rev	1.0
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B			
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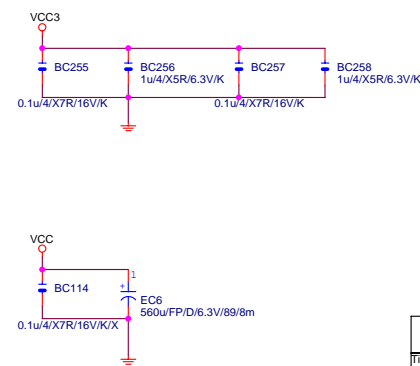
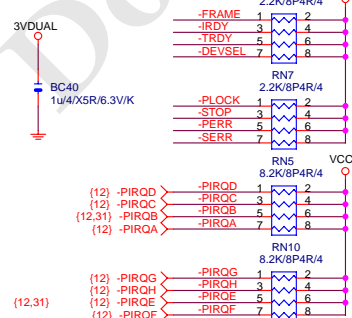
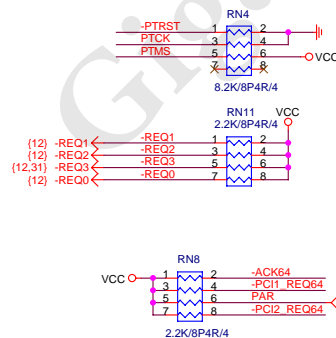
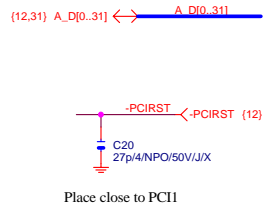
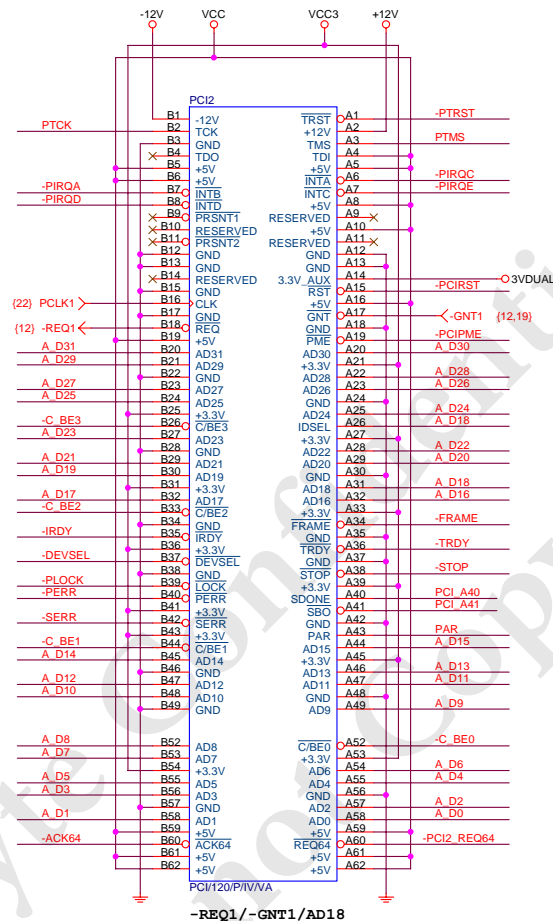
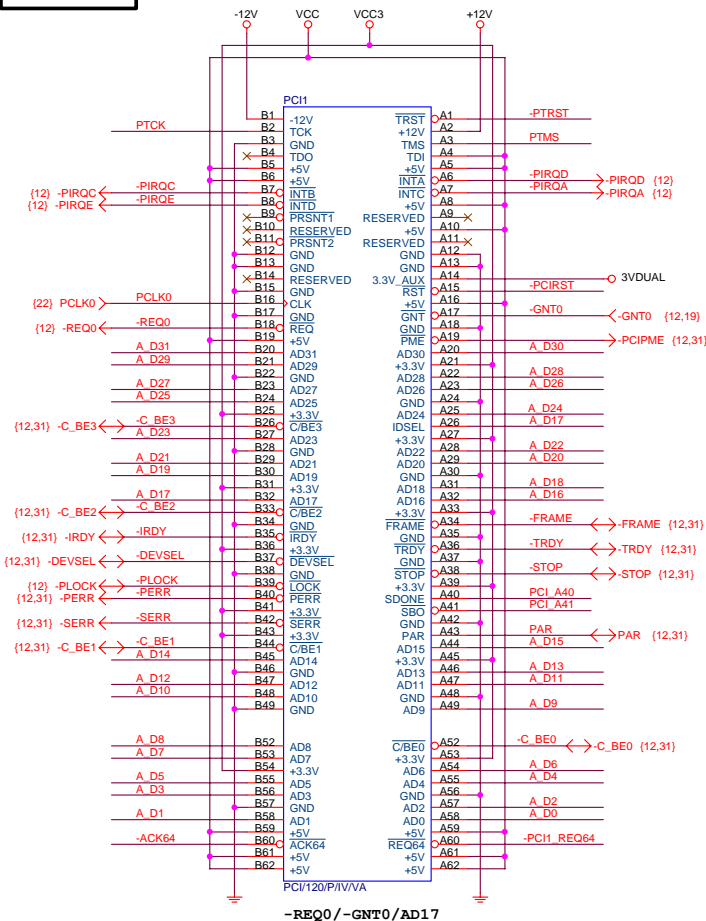


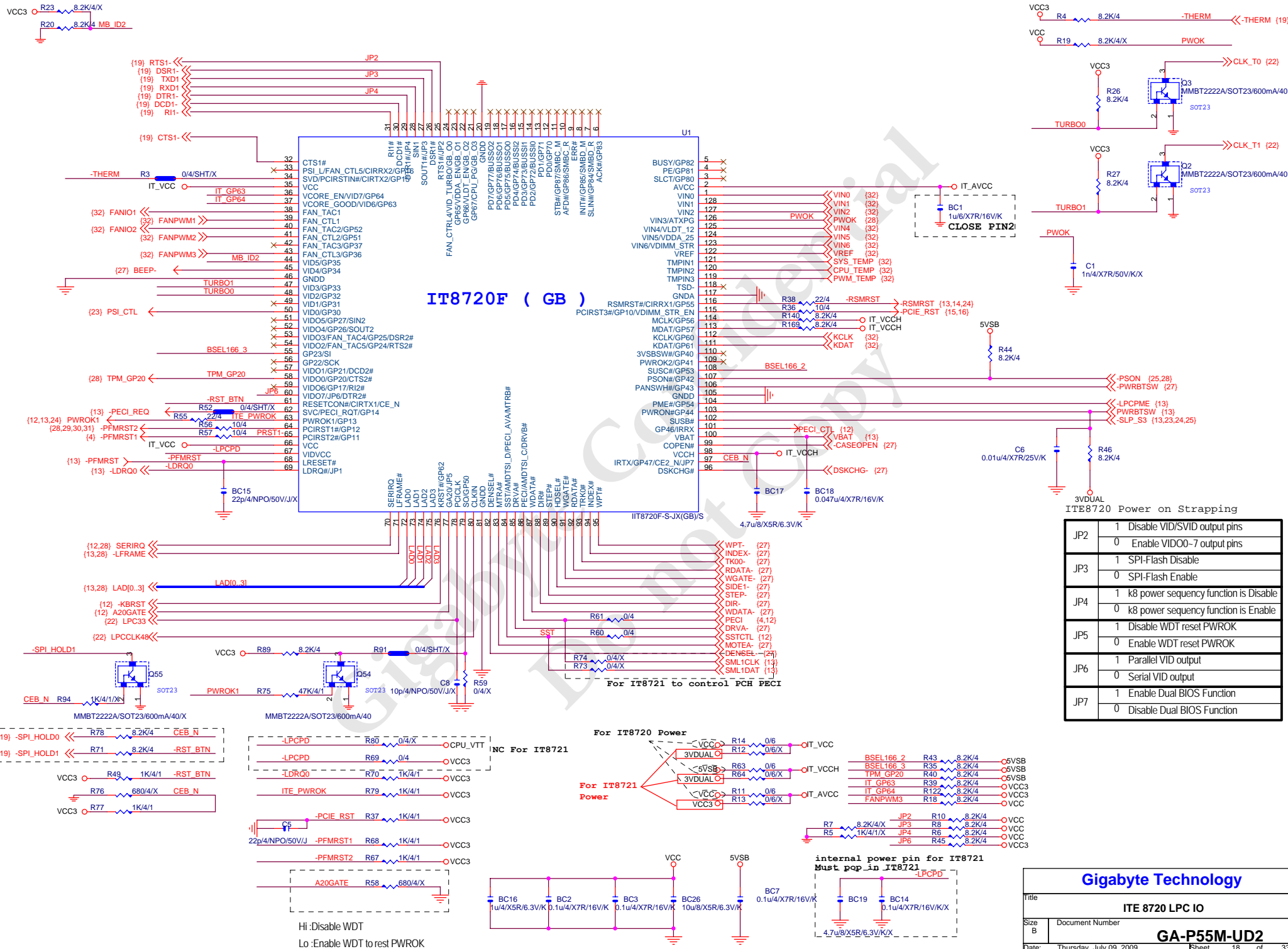


Gigabyte Technology

Title			PCI EXPRESS * 16
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PCI1,2 SLOT



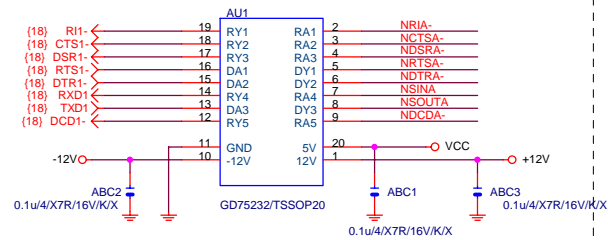


JP2	1	Disable VID/SVID output pins
	0	Enable VID00-7 output pins
JP3	1	SPI-Flash Disable
	0	SPI-Flash Enable
JP4	1	k8 power sequency function is Disable
	0	k8 power sequency function is Enable
JP5	1	Disable WDT reset PWROK
	0	Enable WDT reset PWROK
JP6	1	Parallel VID output
	0	Serial VID output
JP7	1	Enable Dual BIOS Function
	0	Disable Dual BIOS Function

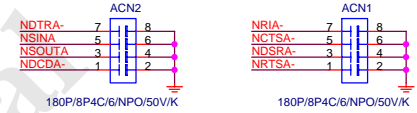
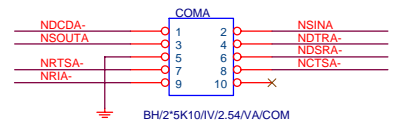
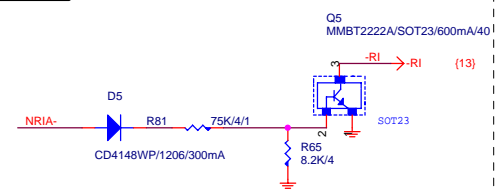
Gigabyte Technology

Title				ITE 8720 LPC IO			
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COMA



COM RI

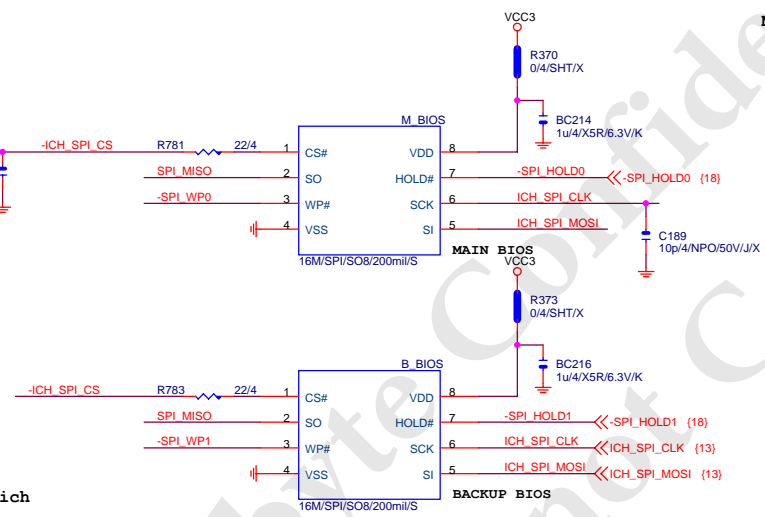


r1.0 DG;0.7 CRB

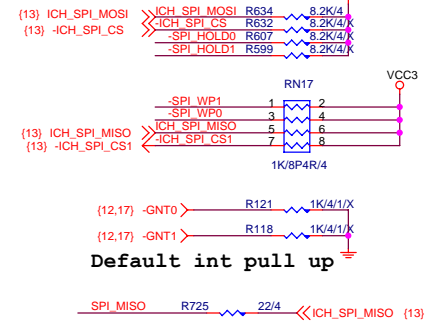
BOOT DEVICE	GNT1	GNT0
LPC	0	0
PCI	0	1
SPI	1	1

1 means floating
0 means PD 1K

IC8SO-SOCKET need to check which is right

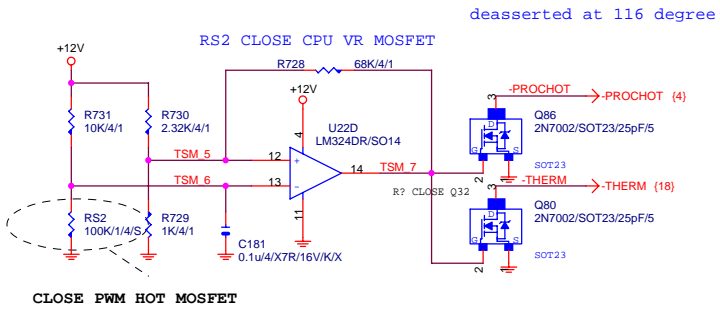
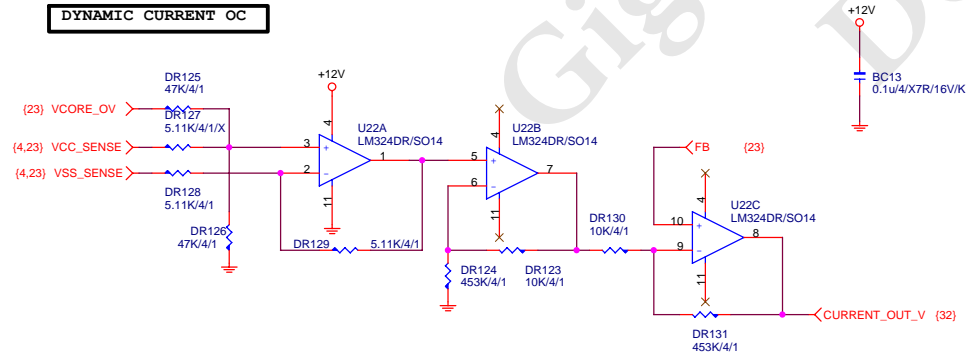


MOSI pull up to enable iTPM , floating to disable



-PROHOT

DYNAMIC CURRENT OC



co-layout

(21) SPDIF02_HDMI

50 Ohm 4/5

VCC3

CR14/CBC4 close to SouthBridge

CR53 2.2/8

CBC37 22u/8/X5R/6.3V/M

CR46 8.2K/4

CR57 8.2K/4

CR58 22/4

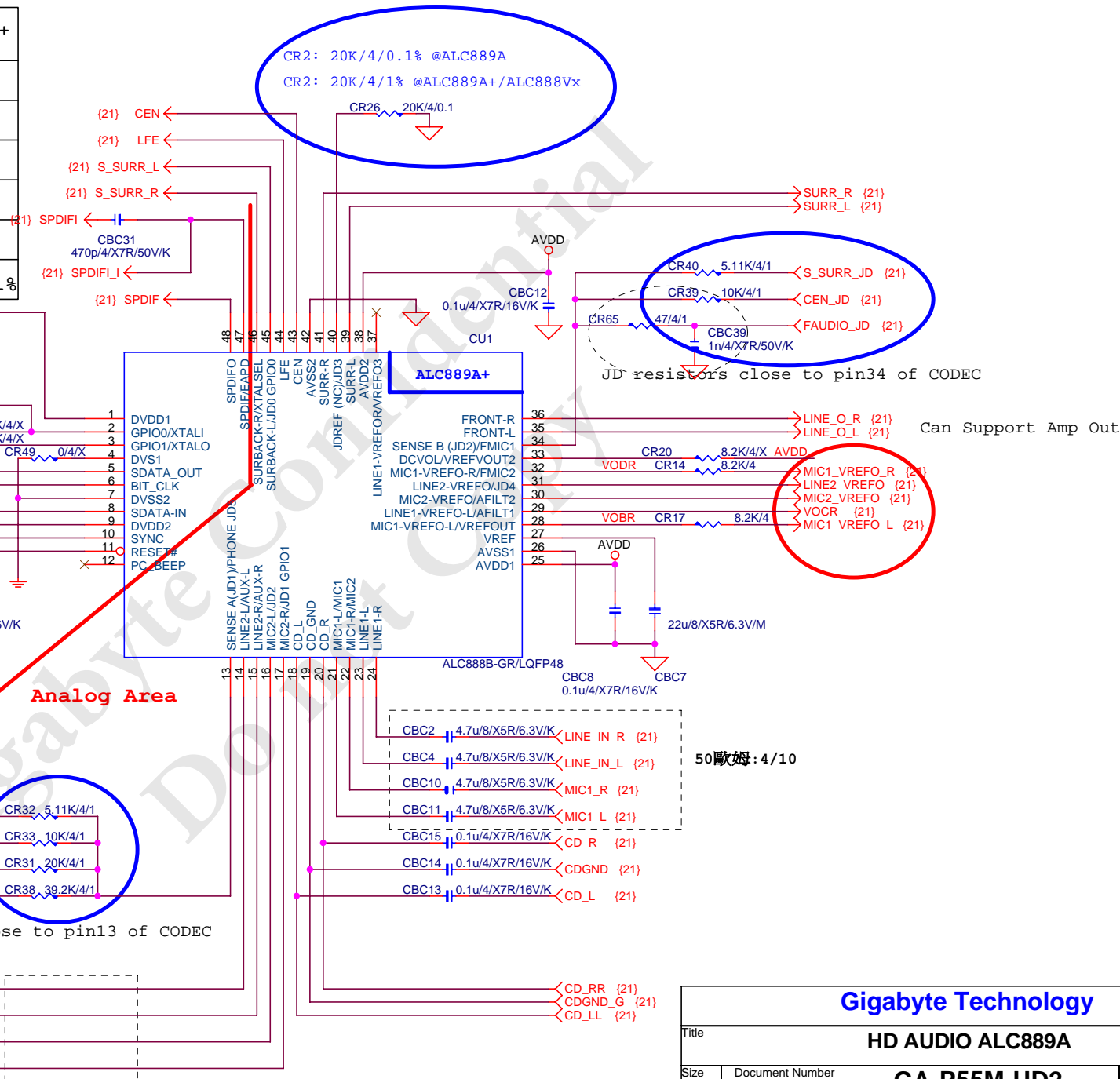
CR59 22/4

CBC34 22p/4/NPO/50V/J/X

CBC35/CBC33

JD resistors close to pin13 of CODEC

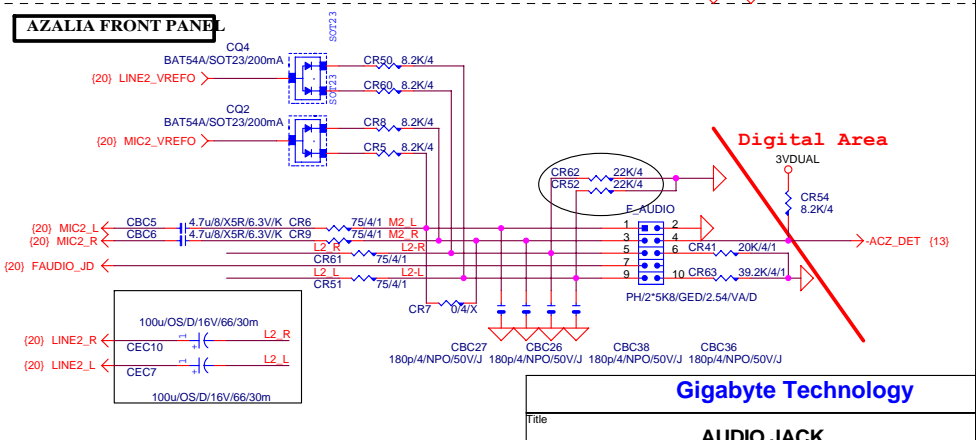
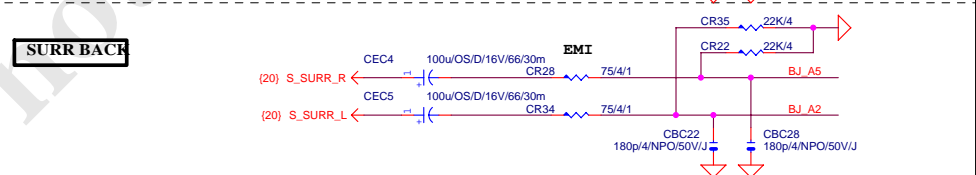
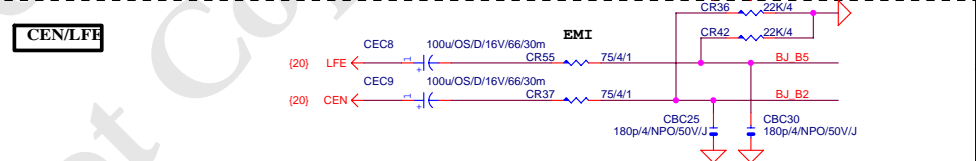
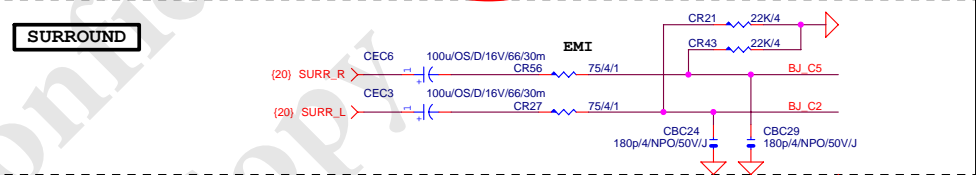
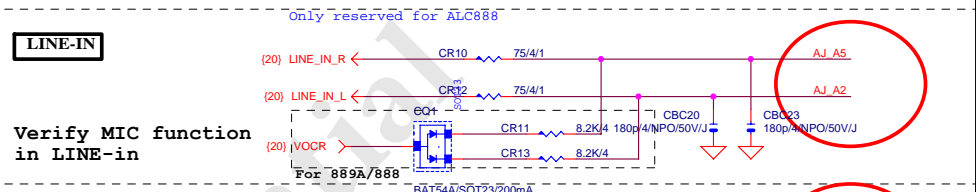
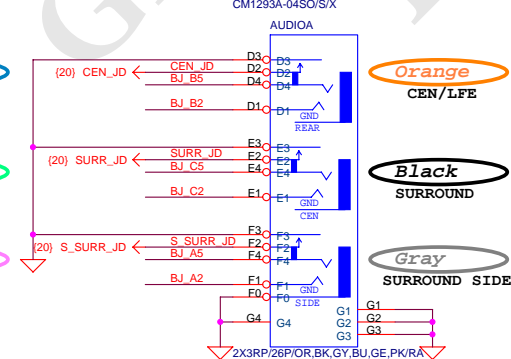
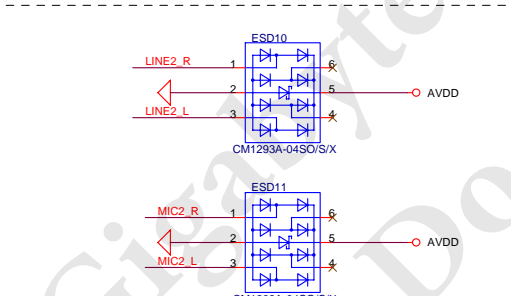
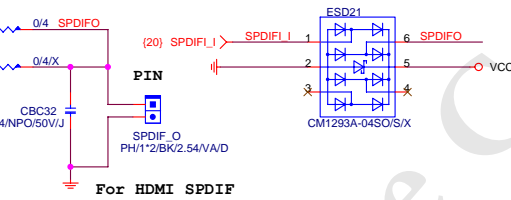
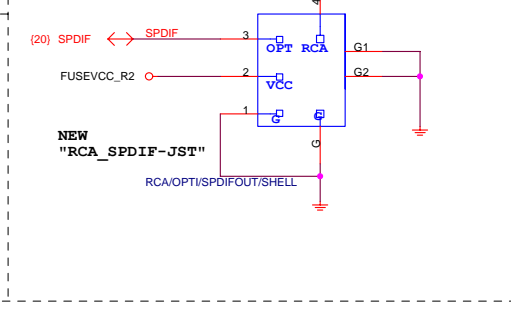
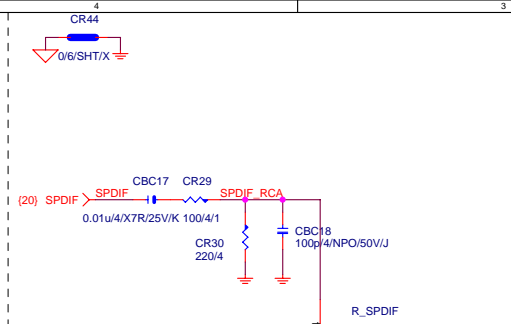
Can Support Amp Out



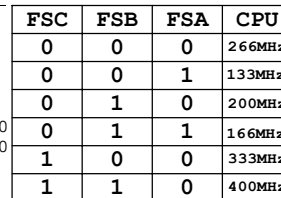
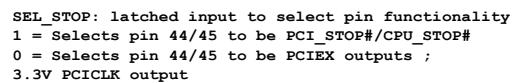
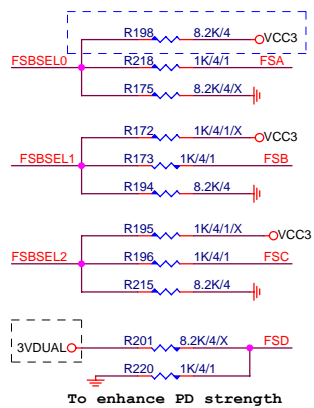
Gigabyte Technology

HD AUDIO ALC889A

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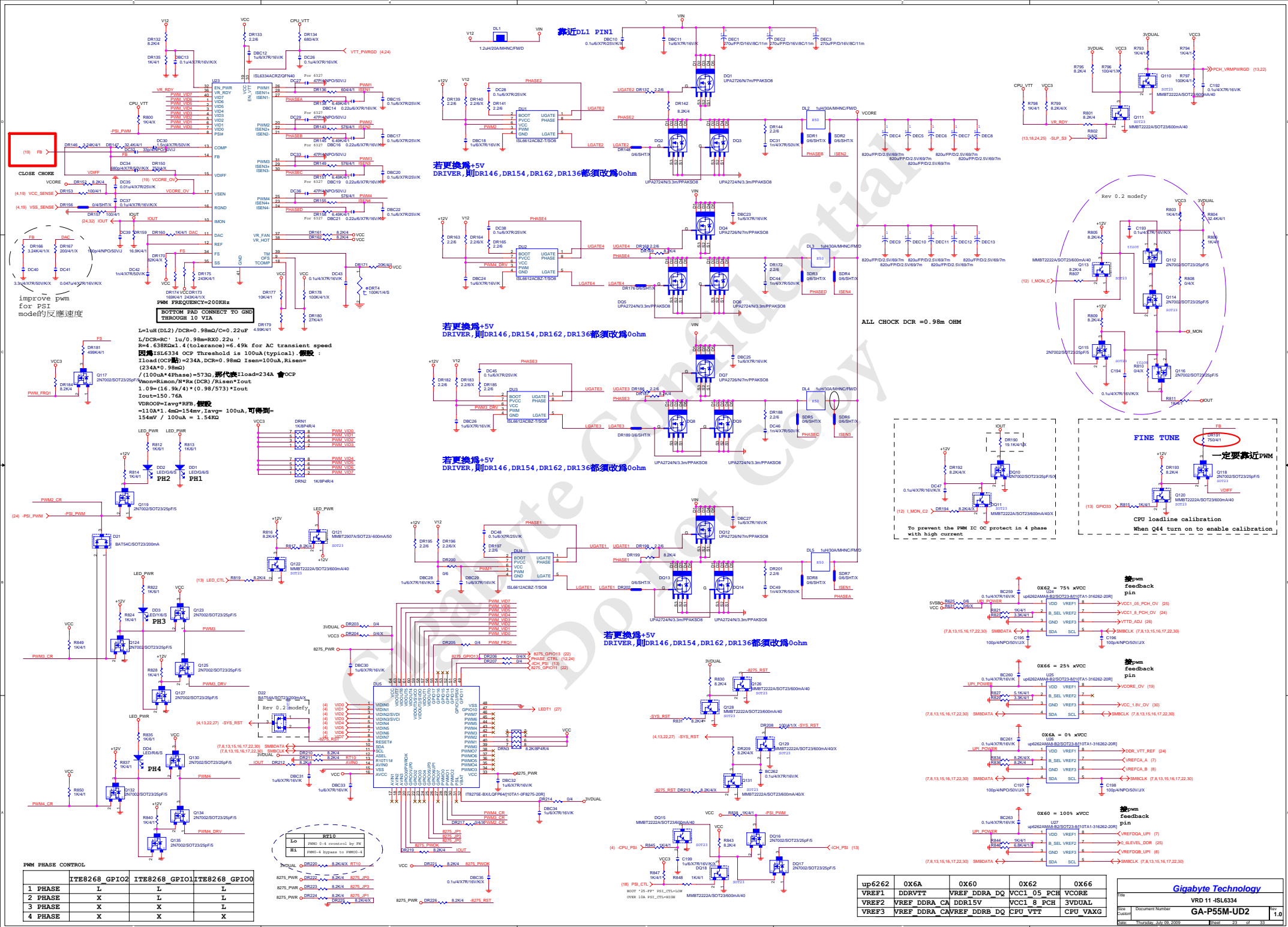


Gigabyte Technology			
Title			
AUDIO JACK			
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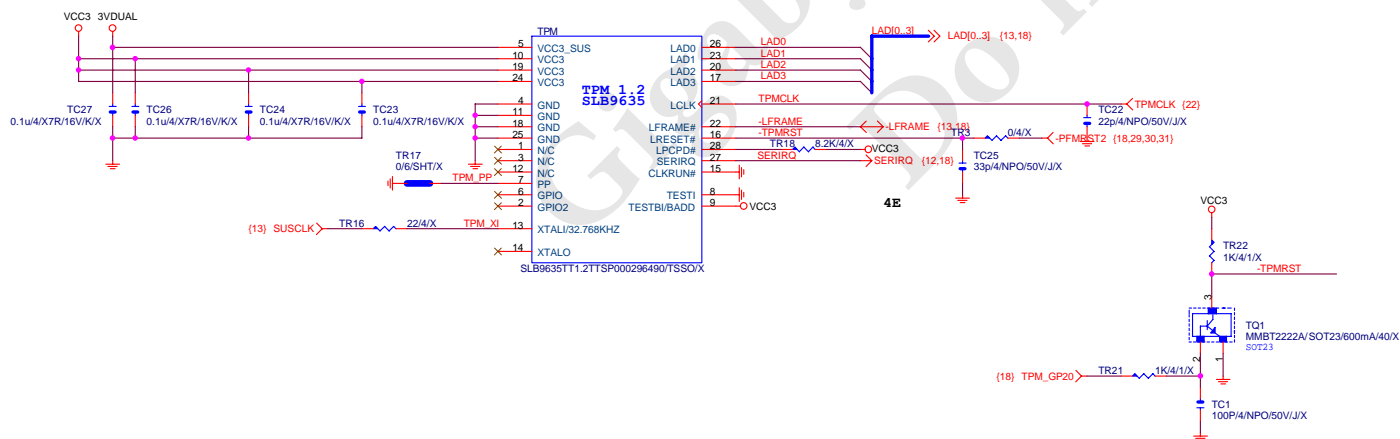
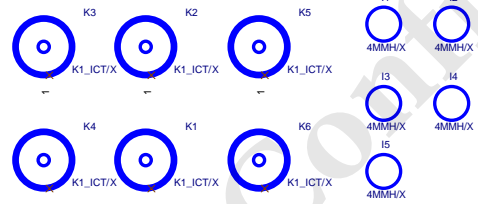
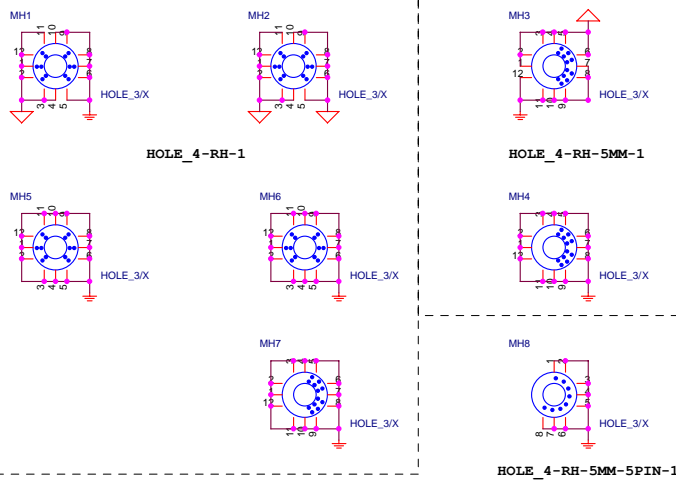
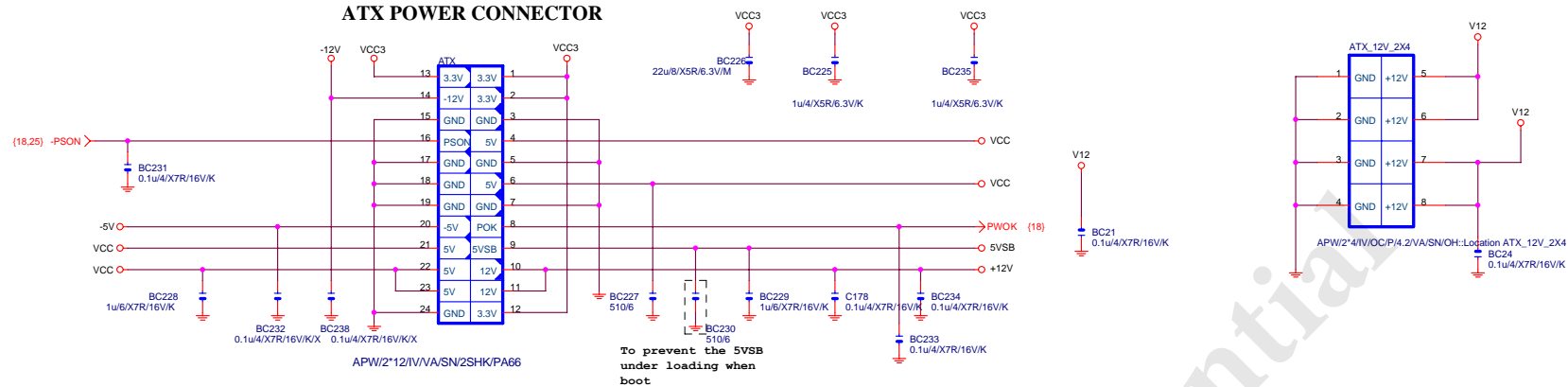


Rev 0.2 modify

Title			
CK505 CLK GEN			
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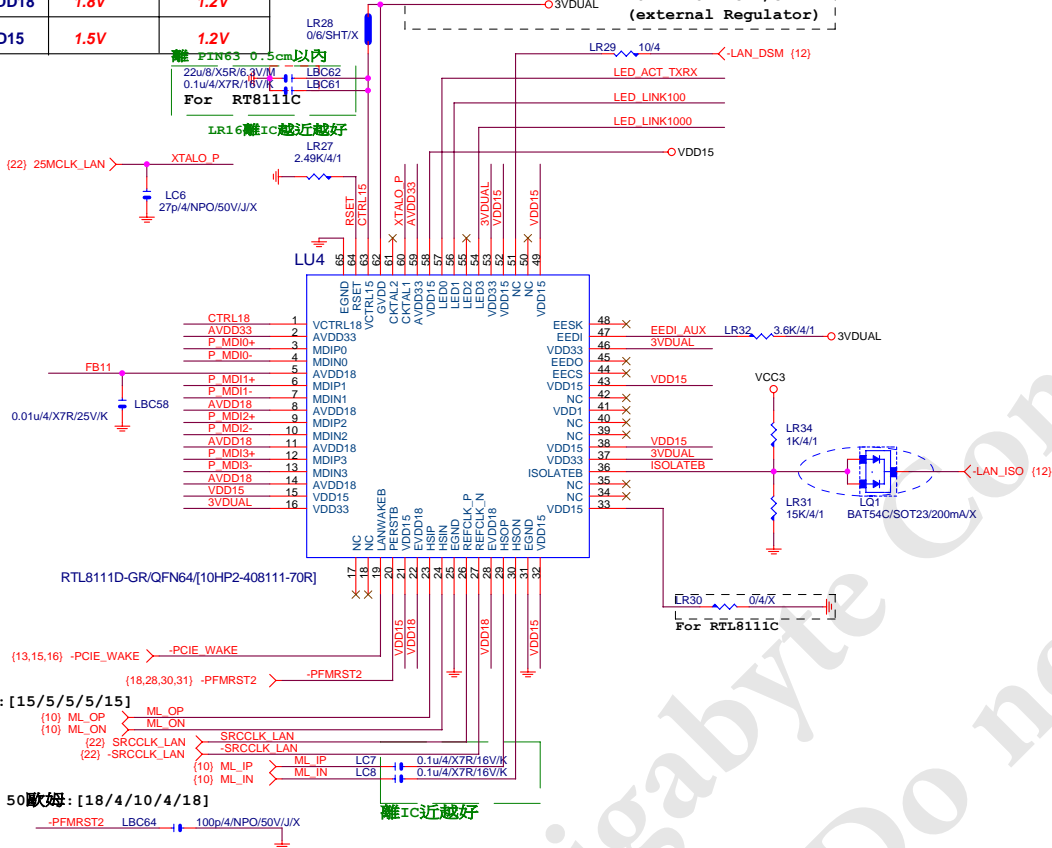
PCIE-1G LAN

Power domain chart

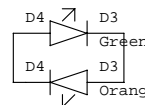
	RTL8111B / RTL8101E	RTL8111C
AVDD33	3.3V	3.3V
AVDD18	1.8V	1.2V
EVDD18	1.8V	1.2V
VDD15	1.5V	1.2V

Pin 63 0.5cm 以內
22u8/X5R/6.3V/M
0.1u4/X7R/16V/K
For RT8111C

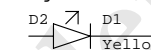
LR16 離IC 越近越好



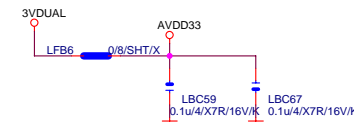
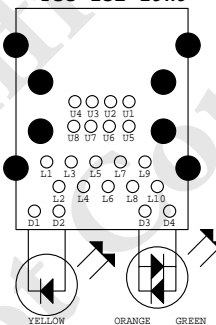
Dual Color LED



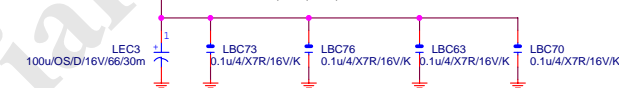
Single Color LED



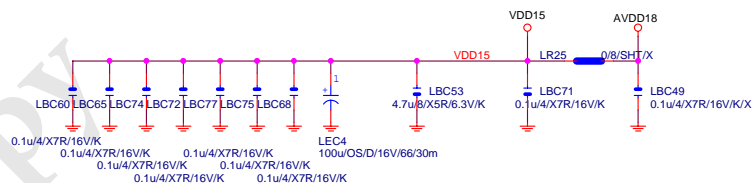
P35-152-19W9



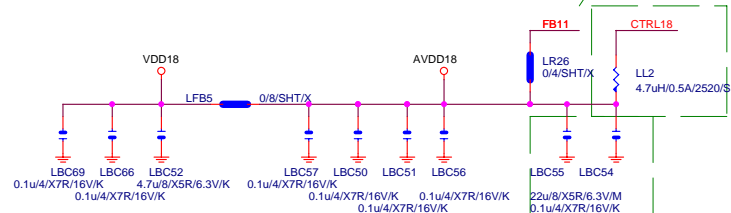
FOR CLOSE PIN1,29,37,40



for RT8111C Mount

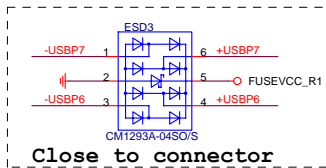


距離pin1 在0.5cm以內



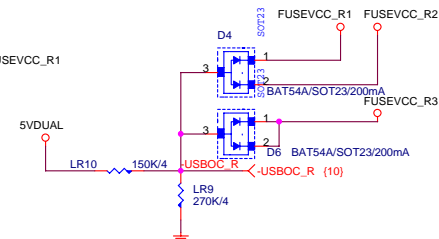
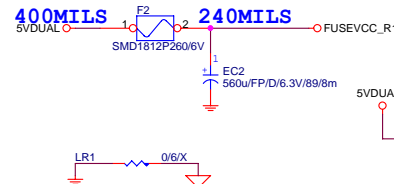
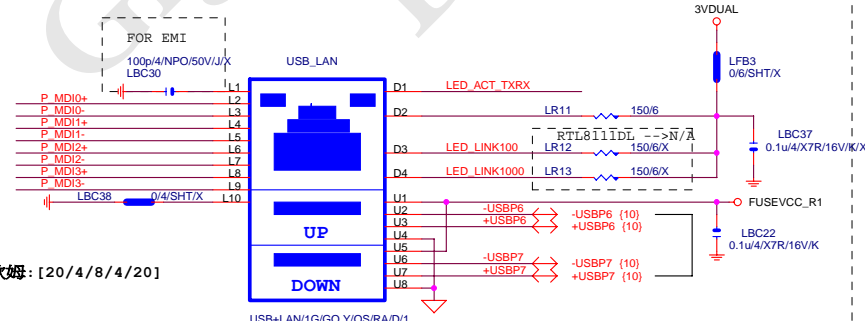
距離LL2 在0.5cm以內

USB LAN CONNECTOR



Close to connector

90 歐姆: [20/4/8/4/20]

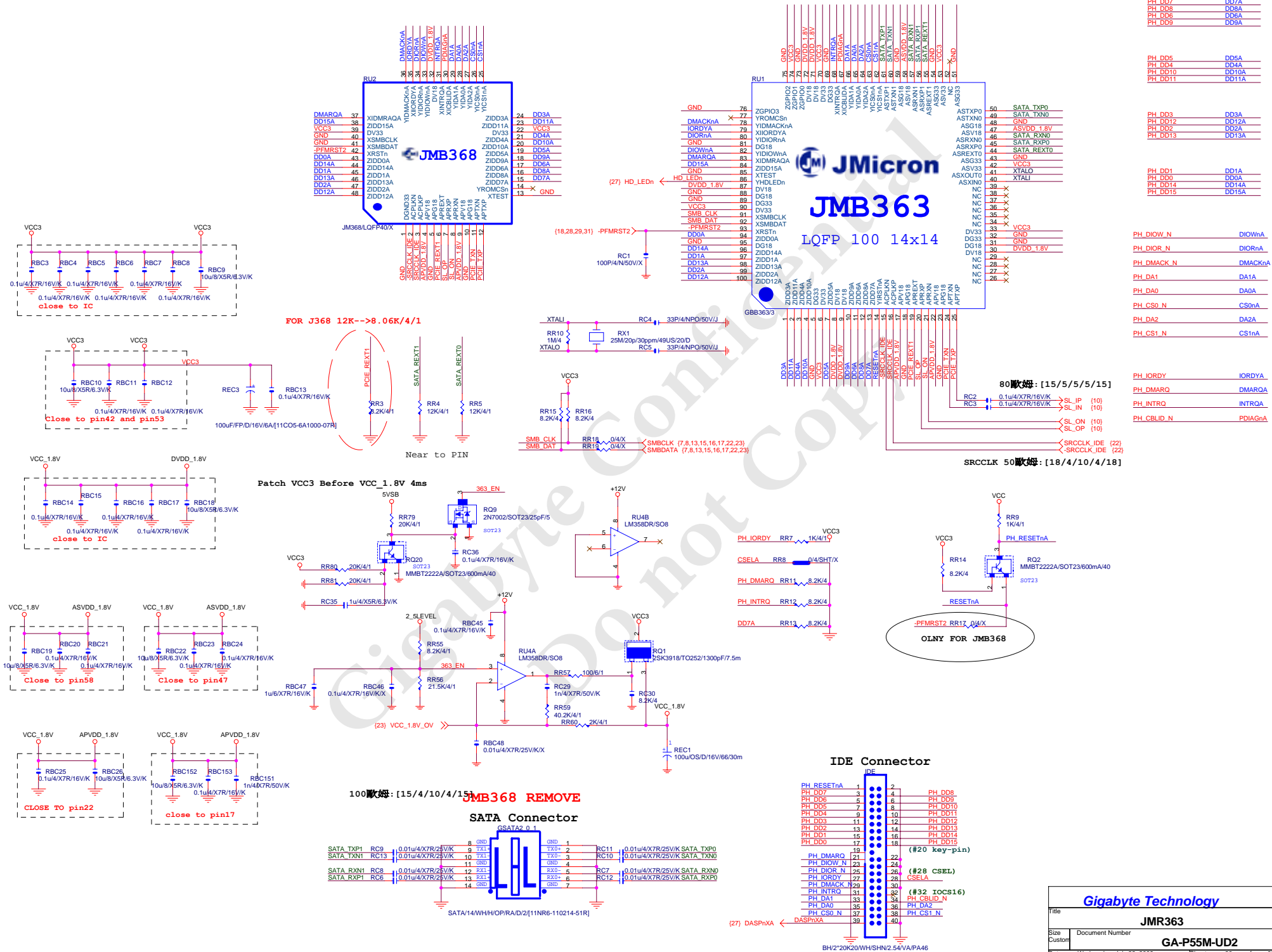


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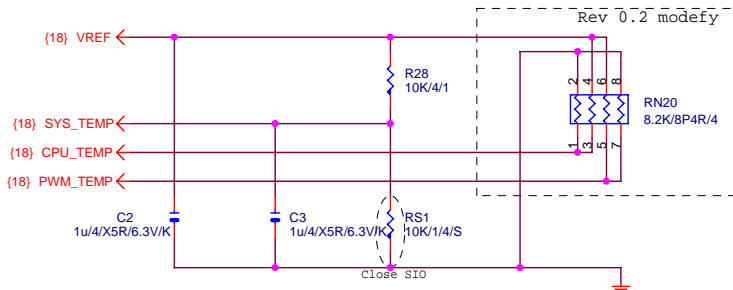
REALTEK RTL8111C

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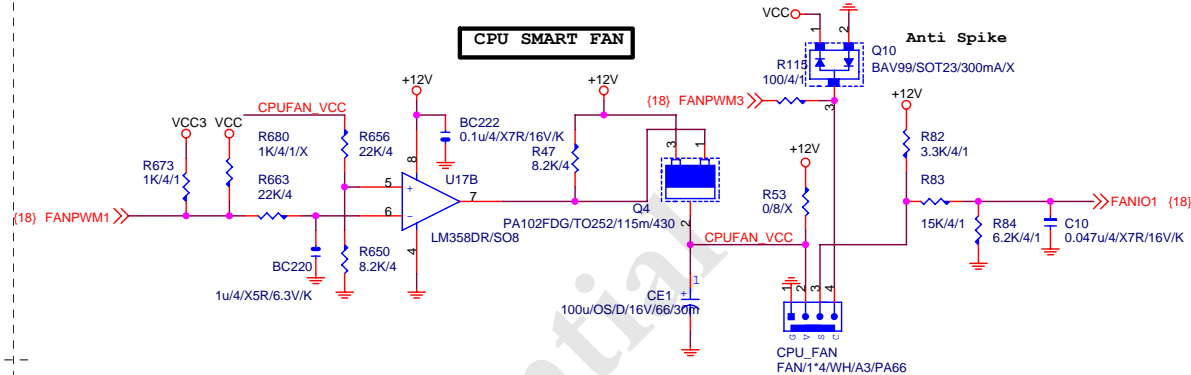
90 歐姆: [15/4.5/7.5/4.5/15]



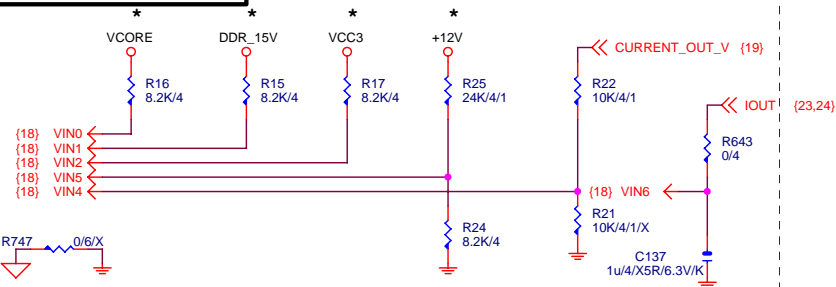
TEMP H/W MONITOR



CPU SMART FAN

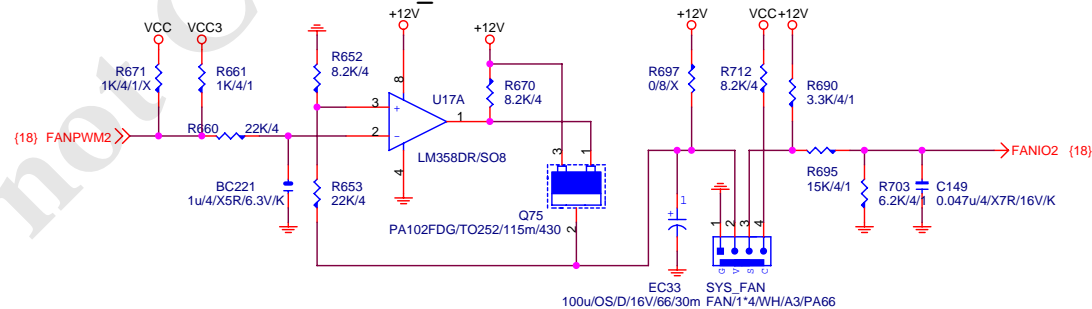


VOLTAGE-- H/W MONITOR

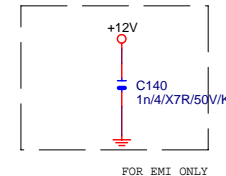
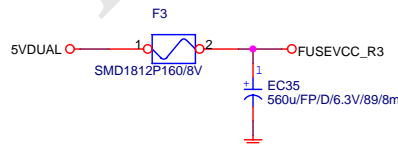
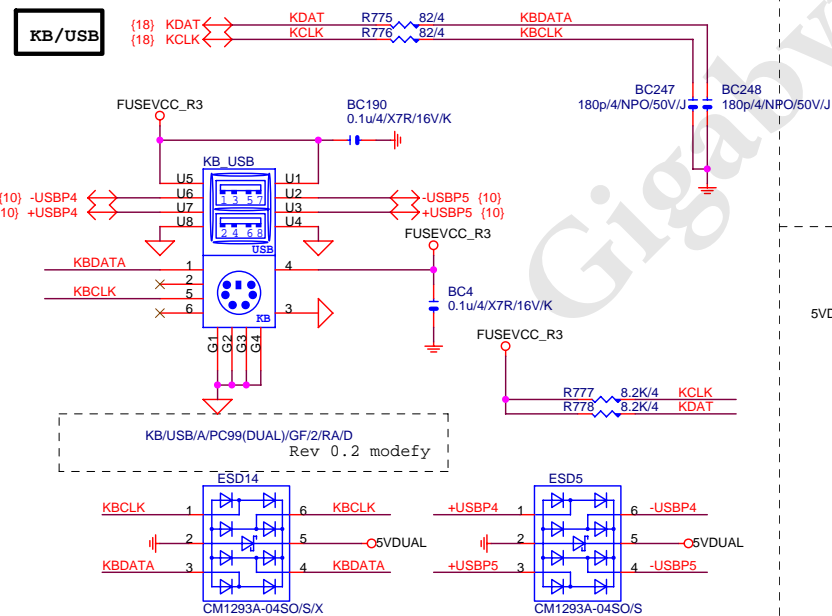


SYS FAN

Linear SYS_FAN



KB/USB



Gigabyte Technology

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